on page 7, line 21, please delete "should be" and insert in its place -- may be a height between the height of the first gate layer and the surface of the substrate. Preferably, the isolation pad height 66 may be less than or equal to ~~the~~

on page 7, line 22, after "306," please insert --or the height of the isolated component 200 (Figure 2H), or for embodiments having only the first gate layer 40 (Figure 2E), less than or equal to approximately one half of the height of the first gate layer 40 (*i.e.* less than or equal to ~~the~~

on page 7, line 22, after "ratio," please insert --). Even more preferably, the field oxide isolation pad height 66 may be small enough to completely prevent the formation of spacers adjacent the field oxide isolation pad ~~66~~

In the Claims:

Please amend the claims as follows:

22. (Amended) A microelectronic device, comprising:

a microelectronic substrate;

a structure including a gate oxide layer formed on the substrate[;] and a first [polysilicon] gate layer formed on the gate oxide layer,[;] the structure having a trench at least partially disposed therein [defined through the polysilicon gate layer, the gate oxide layer] and extending into the substrate; and

a field oxide layer at least partially in the trench, the field oxide layer having a field oxide level between the level of an upper surface of the substrate and the level of an upper surface of the first [polysilicon] gate layer.

23. (Amended) The [A] microelectronic device of claim 22, further comprising:

[a microelectronic substrate;

a gate oxide layer formed on the substrate;

a polysilicon gate layer formed on the gate oxide layer;

a trench defined through the polysilicon gate layer, the gate oxide layer and extending into the substrate;

a field oxide in the trench, the field oxide having a field oxide level between the level of an upper surface of the gate oxide and the level of an upper surface of the polysilicon gate layer;]

a polysilicon [ploysilicon] adhesion layer formed at least partially over the first [polysilicon] gate layer and [the upper surface of] the field oxide layer.

32. (Amended) A microelectronic device, comprising:

a microelectronic substrate having a trench formed in a surface thereof;

a gate structure formed on the substrate; and

a field oxide deposited in the trench, the field oxide extending from the trench beyond the surface of the substrate[,] by a height which is less than or equal to approximately one half of a height of the gate structure formed on the substrate.

Please add the following new claims:

35. The microelectronic device of claim 22 wherein the first gate layer comprises a polysilicon layer.

36. The microelectronic device of claim 22 wherein the field oxide level is less than or equal to approximately one half the distance between the upper surface of the substrate and the upper surface of the first gate layer.

37. The microelectronic device of claim 24 wherein the field oxide level is less than or equal to approximately one half the distance between the upper surface of the substrate and the upper surface of the silicide layer. --

REMARKS

Claims 22-34 are pending in the present application. In the Office Action dated December 9, 1999, the Examiner (1) rejected claims 26-31 under 35 USC § 112, first paragraph, as containing subject matter that was not described in the specification; (2) rejected claims 22, 32, and 34 under 35 USC § 102(b) as being anticipated by Manning (US 5,177,028); and (3) rejected claims 23-25 and 33 under 35 USC § 103(a) as being unpatentable over Applicant's Admitted Prior Art Figure 1 in view of Manning (US 5,177,028).